WHAT IS CLAIMED IS:

1. A method of making an integrated circuit in a semiconductor substrate, the method comprising:

forming at least two isolation regions in the semiconductor substrate;

forming a well between the two isolation regions, the well defining a body region;

forming a first oxide layer above a first portion of the body region;

forming a first dielectric layer above the first oxide layer;

forming a first polysilicon layer above said first dielectric layer, said first polysilicon layer forming a control gate of a non-volatile device;

forming a second dielectric layer above the first polysilicon layer;

forming a first spacer above the body region and adjacent said first polysilicon layer;

forming a second oxide layer above a second portion of the body region not covered by said first spacer;

forming a second polysilicon layer over the second oxide layer, the first spacer and a portion of the second dielectric layer; said second polysilicon layer forming a guiding gate of the non-volatile device and a gate of an MOS transistor;

delivering first implants to the body region to form lightly doped areas in the body region;

delivering second implants to the defined source and drain regions;

forming a second spacer above the body region to define regions receiving lightly dopes implants and to define a conducting region of a capacitor of the non-volatile cell.

2. The method of claim 1 further comprising:

forming a salicide layer over the portions of the lightly doped areas in the body region that form polysilicon landing pads.

3. The method of claim 2 further comprising:

forming a metal layer over the salicide layer to form a bitline and a terminal adapted to receive a supply voltage.

4. The method of claim 3 wherein a doping concentration of the first implants delivered to one of the source and drain regions of the non-volatile device is greater than a doping concentration of the first implants delivered to the other one of the source and drain regions of the non-volatile device.

5. The method of claim 4 wherein said first dielectric layer further includes an oxide layer and a nitride layer.

6. The method of claim 5 wherein said second dielectric layer further includes an oxide layer and a nitride layer.

7. The method of claim 6 wherein said well is a p-well.

8. The method of claim 7 further comprising:

forming an n-well below the p-well.

9. The method of claim 8 wherein said n-well is formed using at least one implant step.

10. The method of claim 9 wherein at least two implant steps are used to form the n-well using a same mask.

11. The method of claim 10 wherein said second oxide layer has a thickness greater than the thickness of the first oxide layer.